Amendments to the claims (this listing replaces all prior versions):

1. (Currently amended) A method comprising:

reducing peak power consumption in a processor which has a future file and which is capable of restoring two or more registers of the future file in a single clock cycle and would do so at a first peak power consumption level, by restoring two or more registers of the future file over more than one clock cycle when a termination occurs in the processor at a second peak power consumption level that is lower than the first peak power consumption level.

2. (Previously Presented) The method of Claim 1, wherein the processor is a pipelined processor.

3. (Previously Presented) The method of Claim 1, wherein restoring two or more registers of the future file comprises updating two or more speculative registers in the future file with architectural values.

4. (Original) The method of Claim 1, wherein more than one clock cycle comprises two clock cycles.

5. (Original) The method of Claim 1, wherein more than one clock cycle comprises three clock cycles.

6. (Previously Presented) The method of Claim 1, wherein the processor is a pipelined processor and more than one clock cycle comprises a number of clock cycles required to flush the processor.

7. (Currently Amended) An apparatus comprising:

a control unit coupled to a first set of registers, a second set of registers and a pipeline, the control unit adapted to restore two or more registers of the first set of registers with data contained in the second set of registers over more than one clock cycle and at a first peak power consumption level following a termination of an instruction in the pipeline although the control unit has the capability of restoring two or more registers of the first set of registers with data contained in the second set of registers in one clock cycle and would do so at a second peak power level that is higher than the first peak power level.

8. (Original) The apparatus of Claim 7, wherein each register in the second set of registers is associated respectively with a register in the first set of registers.

9. (Original) The apparatus of Claim 7, wherein more than one clock cycle comprises two clock cycles.

10. (Original) The apparatus of Claim 7, wherein more than one clock cycle comprises three clock cycles.

11. (Original) The apparatus of Claim 7, wherein the control unit is further adapted to flush the pipeline following the termination of the instruction in the pipeline.

12. (Previously Presented) The apparatus of Claim 11, wherein more than one clock cycle comprises the number of clock cycles required by the processor to flush the pipeline.

13. (Original) The apparatus of Claim 12, the control unit further adapted to restore at least one register in the first set of registers after the pipeline has been flushed.

14. (Original) The apparatus of Claim 7 wherein the pipeline is an X-stage pipeline, the control unit adapted to restore the first set of registers with data contained in the second set of registers over X-N clock cycles or fewer, following a termination of an instruction in an N^{th} stage of the pipeline.

15. (Currently Amended) A system comprising:

a static random access memory device;

a processor coupled to the static random access memory device, wherein the processor includes a first set of registers, a second set of registers, a pipeline and a control unit adapted to restore two or more of the registers in the first set of registers with values in the second set of registers over more than one clock cycle and at a first peak power consumption level if a termination occurs in the pipeline although the processor is capable of restoring the first set of registers with values in the second set of registers in one clock cycle and would do so at a second peak power consumption level that is higher than the first peak power level.

16. (Original) The system of Claim 15, wherein more than one clock cycle comprises two clock cycles.

17. (Original) The system of Claim 15, wherein more than one clock cycle comprises three clock cycles.

18. (Original) The system of Claim 15, wherein the control unit is further adapted to flush the pipeline following the termination of the instruction in the pipeline.

19. (Previously Presented) The system of Claim 18, wherein more than one clock cycle comprises the number of clock cycles required by the processor to flush the pipeline.

20. (Original) The system of Claim 19, the control unit further adapted to restore at least one register in the first set of registers after the pipeline has been flushed.

21. (Original) The system of Claim 15, wherein the pipeline is an X-stage pipeline, and wherein the control unit is adapted to restore the first set of registers with data contained in the second set of registers over X-N clock cycles or fewer, following a termination of an instruction in an N^{th} stage of the pipeline.